REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on December 6, 2001, and the references cited therewith.

Claims 44 and 47 are amended and claims 53, 60, and 61 are canceled; as a result, claims 38-52, 54-59, and 62-79 are now pending in this application.

Information Disclosure Statement

For the Examiner's convenience, applicant has included copies of the crossed-out references from the Information Disclosure Statement filed December 21, 2000 and a clean copy of the Form 1449. Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted, marked as being considered and initialed by the Examiner, be returned with the next official communication.

Election/Restrictions

Claims 53 and 60-61 have been withdrawn from consideration. Applicant reserves the right to introduce them in a future continuin application.

Double Patenting Rejection

Claims 38-52, 54-59, and 62-79 were rejected under the judicially created doctrine of double patenting over claims 1-19 of U.S. Patent No. 5,923,584.

Applicant will submit a suitable Terminal Disclaimer in due course after the issues of patentability have been resolved as to the remaining claims.

§112 Rejection of the Claims

Claims 44, 47, 62, 63, 68, and 69 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Independent claims 44 and 47 have been amended so that they and their dependent claims 62, 63, 68 and 69 are no longer indefinite.

§103 Rejection of the Claims

Claims 38-52, 54-59, and 62-79 were rejected under 35 USC § 103(a) as being unpatentable over Nihira et al. (U.S. Patent No. 4,908,324).

The Nihira et al patent relates to a method for making a bipolar transistor. The Office Action, in rejecting the claims under 35 USC § 103(a) only, concedes that Nihira et al does not show each and every element of the claims, arranged as shown in the claims. In contrast, each of the rejected claims is drawn to "an intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer".

Applicant maintains that the preamble to the claims is relevant to the applicability of the cited Nihira et al patent to the claims. In considering the differences between what is shown in the cited Nihira patent and the claims, the question under 35 U.S.C. 103 is not whether those differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985); MPEP § 2141.02. Applicant submits that the present office action fails to establish a *prima facie* case of obviousness of the claimed invention, taken as a whole, of the rejected claims.

Applicant also traverses the fact that the Office Action based certain assertions made in support of the rejection on the taking of "Official Notice".

The Office Action took official notice that "the use of photoresist is well known in the art as a maeans of patterning structures in the semiconductor industry and would be obvious to form the resist, as recited, as part of a conventional multilevel interconnect process to enable formation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit".

The Office Action also took official notice that "As is well known as a dopant and it would have been obvious to switch the dopant types of the structure to provide greater process and device latitude". Additionally the Office Action states: "Further, it would be obvious and is well known to use As as an N-type dopant".

The Office Action took furrther official notice that ".... it would be obvious to employ an etch stop layer in an etch-back planarization process, as recited, as part of a conventional multilevel interconnected process to enable formulation of interconnects and bond pads necessary to incorporate the disclosed device in an integrated circuit." Additionally, the Office Action asserted "It is well known to employ an etch stop over a structure that one would like to protect during an etching process so as not to overetch the structure, causing it damage". Finally the Office Action further stated "...the use of Ti silicide as an etch stop material is also well known in the art and would be obvious to use in a conductive poly structure in order to both stop an etch and to further increase the conductivity of the structure."

Applicant respectfully traverses each and every one of the instances where the Office Action takes official notice and hereby requests the Examiner to provide references that describe such elements. Absent identification of such references, it would appear that the Examiner is using personal knowledge, so, in any such instances, the Examiner is respectfully requested to submit the affidavit required by 37 C.F.R. § 1.104(d)(2).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.* Here, because of the frequent use of "Official Notice" as to many elements of rejections in the present Office Action, the Office Action does not appear to meet the requirements of 35 U.S.C. § 103 to establish a *prima facie* case of obviousness.

At a minimum, the Office Action also fails to show how Nihira, which consistently shows a structure where polycrystalline silicon layer 11 does not have a thickness selected "such that the lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region" where oxide region 8 extends above the upper surface of silicon layer 11.

Applicant reserves the right to further demonstrate how the prior art may not properly be combined to show what is claimed in claims 38-52 and 62-79. Reconsideration and withdrawal of the improper rejection under 35 U.S.C. § 103 and allowance of the pending claims is

respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6970 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

MARTIN CEREDIG ROBERTS ET AL.

By their Representatives,

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Date 2/22/2002 By _____
Charles E. Steffey
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 22nd day of February, 2002.

Tina Pugh
Name

Signature

Docket No. 303.451US6
WD # 418539

Micron Ref. No. 93-0512.05

CLEAN VERSION OF PENDING CLAIMS

METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS
Applicant: Martin Ceredig Roberts et al.
Serial No.: 09/745,780

Claims 38-52, 54-59, and 62-79, as of February 22, 2002 (Date of Response to First Office Action).

38. An intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide regions but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region; and

a second polycrystalline silicon layer overlying the first polycrystalline silicon layer and the first substrate region.

39. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

41. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the field oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

44. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

45. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second

substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the field oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

46. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region.

47. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

48. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region including a field oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region including a field oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a gate oxide region, overlying at least a portion of the second

substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the field oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region, including a field oxide region, overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the field oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

54. The intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

55. The intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

56. The intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

57. The intermediate of claim 56 wherein the first and second polycrystalline silicon layers are doped with arsenic.

58. The intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

59. The intermediate of claim 58 wherein the first and second polycrystalline silicon layers are doped with arsenic.

62. The intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

63. The intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

64. The intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

65. The intermediate of claim 64 wherein the polycrystalline plug and the polycrystalline silicon layer are doped with arsenic.

66. The intermediate of claim 46 wherein the polycrystalline plug is doped to increase its conductivity.

67. The intermediate of claim 66 wherein the polycrystalline plug is doped with arsenic.

68. The intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

69. The intermediate of claim 68 wherein the first and second polycrystalline silicon layers are doped with arsenic.

70. The intermediate of claim 48 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

71. The intermediate of claim 70 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

72. The intermediate of claim 49 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

73. The intermediate of claim 72 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

74. The intermediate of claim 50 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

75. The intermediate of claim 74 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

76. The intermediate of claim 51 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

77. The intermediate of claim 76 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.

78. The intermediate of claim 52 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped to increase their conductivity.

79. The intermediate of claim 78 wherein the first polycrystalline silicon layer and the polycrystalline silicon plug are doped with arsenic.